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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,830	01/30/2001	Frank K. Baker JR.	SC11150TH	2027

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EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/772,830	BAKER ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10 and 12-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10 and 12-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In view of the supplemental appeal brief filed on 14 April 2006, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below (see end of Office action):

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-10, 12-14, 16-18, and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter AAPA) in view of Okuno (US Patent #6,105,114).

With respect to independent claims 1, 6, 14, 16, 22, and 25, using claim 1 as representative, a memory system is disclosed by AAPA in prior art figure 1, e.g.

An array of addressable storage elements arranged in a plurality of rows and columns, wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells is disclosed in figure 1, and discussed in the instant specification at page 1.

Decoding circuitry as claimed is disclosed in prior art figures 1 and 9, and discussed on pages 1 and 2 of the instant specification. See page 2, "consecutive addresses are associated with memory cells arranged along the same row of memory array 110." Also see figure 9, A11-A16, which describes the row in the address.

The first [element?] address comprising a group of bits, wherein the second address comprises a group of bits, wherein the decoding circuitry includes a row decoder and a column decoder, wherein the row decoder is operable responsive to a first portion of the group of bits of the first address and the second address, wherein the

column decoder is operable responsive to a second portion of the group of bits of the first address and the second address is disclosed in figures 1 and 9, as well as discussed on pages 1 and 2 of the instant specification. See columns 902 in figure 9 for the "second portion," e.g.

The difference between AAPA and the instant claims is the explicit recitation of a bit of the second portion being more significant than a bit of the first portion.

However, Okuno discloses just such an address transposition in column 5, lines 4-14, and even more specifically in column 8, lines 1-24 and 49-63, as well as in column 9, lines 1-25, and column 11, lines 1-30. "More significant" is interpreted by examiner to be a recognized expression in the state of the art at the time of the instantly claimed invention to denote the bit placements of addresses. For example, there are "MSB's" and "LSB's," or "most significant bits" and "least significant bits," respectively, as recognized in the state of the art at the time of the invention. In Okuno, these are consistently referred to as "lower" and "higher" bits.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of AAPA and Okuno before him/her, to modify the prior art system of AAPA to transpose the addresses (thereby switching the most and least significant bits of the address) as in Okuno, because it will reduce circuit scale as well as power consumption, as discussed in Okuno at column 4, lines 7-9, e.g.

These two references are analogous as they both deal with memory access and control.

With respect to claims 2 and 8, each storage element storing one bit is inherent – that is what a storage element does, by definition.

With respect to claims 3 and 9, figure 9 of AAPA discloses each of the storage elements storing a word.

With respect to claims 4 and 10, figure 9 of AAPA also discloses each of the storage elements storing bits arranged as a page.

With respect to claim 23, Okuno discloses each bit of the second portion being more significant than each bit of the first portion in column 8, lines 1-24, e.g.

With respect to claim 7, the input of the storage elements being a control gate and the output being a drain are inherent characteristics of floating gate non-volatile memories, as discussed at page 1 of the instant specification, e.g. The whole reasons a floating gate transistor even stores data is because the charge is held or not held on the floating gate – that charge or no charge is what goes through the drain to the sense amps to determine whether a binary"1" or "0" is stored in each cell.

With respect to claim 12, each of the nonvolatile memory cells comprising a floating-gate type cell is disclosed by AAPA on page 1 of the instant specification, e.g.

With respect to claim 13, the at least one of the least significant bits comprising all of the less significant bits is disclosed by Okuno as discussed supra with respect to claim 23, e.g.

With respect to claim 21, Okuno discloses the claimed subject matter as discussed supra with respect to claim 1, e.g.

With respect to claim 26, at least one bit of the group of bits being representative of addresses of a plurality of blocks is disclosed in prior art figure 9, e.g.

With respect to claims 17 and 18, the claimed subject matter is disclosed in prior art figure 9 as well.

With respect to claim 24, Okuno discloses the claimed subject matter as discussed supra with respect to at least claim 1, e.g.

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (cited supra), Okuno (cited supra) as applied to claim 16 above, and further in view of Microsoft Press Computer Dictionary, Third Edition, hereafter MPCD.

The combination of AAPA and Okuno teach the limitations of claim 16, upon which the instant claims depend, as discussed supra.

The difference between the instant claims and the explicit teachings of AAPA and Okuno, is the explicit mention and teaching of burst operations.

However, MPCD teaches that a burst is carried out in a burst mode, which facilitates a "high-speed transfer of data," as disclosed on page 67, e.g.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of AAPA, Okuno, and MPCD before him/her, to modify the system of AAPA and Okuno to include bursting operations as taught by MPCD, in order to facilitate high-speed transfer of data, as disclosed by MPCD on page 67, and which is also well-known to those of even rudimentary skill in the art as a motivation for most memory access systems.

Claims 1-2, 6-8, 12-14, 16, and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno (cited supra) and Ma et al (US Patent #5,933,368).

With respect to claims 1, 6, 14, 16, 22, and 25, taking claim 1 as representative, as noted in the previous Office action prior to the instant Appeal Brief, Okuno teaches all of the claimed limitations as discussed in detail therein (see figures 5, 9, 11A-B, as well as column 7-8, lines 65-8 and column 8, lines 13-25, e.g.), with the exception of explicitly disclosing a non-volatile memory, as also noted in that previous rejection. Okuno discloses using "a memory," but does not specifically state that it is a non-volatile memory (nor does it specify a volatile memory, for that matter).

Ma et al, however, disclose using a non-volatile, floating gate memory in column 1, lines 20-40, e.g.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Okuno and Ma et al before him/her, to use a non-volatile memory as the memory in the system of Okuno, because it is light in weight, occupies very little space, and consumes less power, as discussed in column 1, lines 26-27 of Ma et al.

With respect to claims 2 and 8, each element storing a bit is inherent in storage.

With respect to claim 23, Okuno discloses each bit of the second portion being more significant than each bit of the first portion in column 8, lines 1-24, e.g.

With respect to claim 7, the input of the storage elements being a control gate and the output being a drain are inherent characteristics of floating gate non-volatile

memories, as discussed at page 1 of the instant specification, e.g. The whole reasons a floating gate transistor even stores data is because the charge is held or not held on the floating gate – that charge or no charge is what goes through the drain to the sense amps to determine whether a binary"1" or "0" is stored in each cell.

With respect to claim 12, each of the nonvolatile memory cells comprising a floating-gate type cell is disclosed by Ma et al in column 1, e.g.

With respect to claim 13, the at least one of the least significant bits comprising all of the less significant bits is disclosed by Okuno as discussed supra with respect to claim 23, e.g.

With respect to claim 21, Okuno discloses the claimed subject matter as discussed supra with respect to claim 1, e.g.

With respect to claim 24, Okuno discloses the claimed subject matter as discussed supra with respect to at least claim 1, e.g.

With respect to claim 26, blocks are inherently present in a flash memory such as that of Ma et al – is a flash memory, by definition.

Claims 3-4, 9-10, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno (cited supra) and Ma et al (cited supra) as applied to claims 1, 6, and 16 above, and further in view of MPCD (cited supra), with AAPA (cited supra) offered as evidence of inherency.

With respect to claims 3-4 and 9-10, Okuno and Ma et al teach all of the claim limitations of the claims upon which the instant claims depend, except they lack explicit recitation of the memory having words and pages.

However, MPCD on page 510 defines a "word" as the largest amount of data that can be handled by a microprocessor in one operation, and is also, as a rule, the width of the main data bus. Word sizes of 16 bits and 32 bits are most common. Accordingly, as would be clear to anyone with been rudimentary skill in the art at the time of the invention, the system must have words of some kind, and their size is clearly a design choice.

On page 349, MPCD describes a page as a fixed-size block of memory (which, examiner notes, is how Ma et al describe a flash memory – as using of fixed blocks). When used in the context of a paging memory system, a page is block of memory whose physical address can be changed via mapping hardware, such as the transposition circuitry of Okuno, e.g.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Okuno, Ma et al, and MPCD before him/her, to incorporate the word and page schemes of MPCD into the system of Okuno and Ma et al, as the combination uses flash memory which operates in blocks anyway, and a word size of some kind must inherently be in any system, as made hackneyed in the state of the art. AAPA figure 9 is offered as evidence of being admittedly hackneyed in the state of the art, as it shows both pages and words in the prior art address.

With respect to claims 19-20, The combination of Ma et al and Okuno teach the limitations of claim 16, upon which the instant claims depend, as discussed supra.

The difference between the instant claims and the explicit teachings of Ma et al and Okuno, is the explicit mention and teaching of burst operations.

However, MPCD teaches that a burst is carried out in a burst mode, which facilitates a "high-speed transfer of data," as disclosed on page 67, e.g.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Ma et al, Okuno, and MPCD before him/her, to modify the system of Ma et al and Okuno to include bursting operations as taught by MPCD, in order to facilitate high-speed transfer of data, as disclosed by MPCD on page 67, and which is also well-known to those of even rudimentary skill in the art as a motivation for most memory access systems.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571.272.4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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